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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Edwin H. Taylor
Blakely, Sokoloff, Taylor & Zafman LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,432	SNYDER ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly added limitation in claims 1, 10 and 18, "the sequencer to sequence data to only the arithmetic unit," was not described in the specification to comply with the written description requirement. The Sequencer appears to sequence data to the arithmetic unit as well as the CAE memory and the Data router, as illustrated in Figure 4. Examiner cannot find any support in the disclosure as originally filed for the sequencer ONLY sequencing data to the arithmetic unit. Claims 2-9, 22-17, and 19-26 are rejected for incorporating the defects of claims 1, 10, and 18. Appropriate correction is required.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The newly added limitation in claims 1, 10 and 18, "the sequencer to sequence data to only the arithmetic unit," is unclear because according to the claims each of the plurality

of CAEs includes a sequencer and an arithmetic unit. The claims effectively define a plurality of sequencers and a plurality of arithmetic units. It is unclear which specific sequencer of the plurality of sequencers sequences data to which specific arithmetic unit of the plurality of arithmetic units. Claims 2-9, 22-17, and 19-26 are rejected for incorporating the defects of claims 1, 10, and 18. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-13, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloutier, US Patent 5,892,962, in view of Taylor et al., US Patent 5,603,043 and Pechanek et al., US Patent 5,682,491.

7. Referring to claim 1, Cloutier has taught a re-targetable communication processor, comprising:

a. a connectivity unit (Figure 1, element 106);

b. a digital signal processing core coupled to the connectivity unit (Figure 1, element 104, one of the FPGA's is a digital signal processor);

c. a plurality of scaleable functional units, coupled to the connectivity unit, to execute mathematically intensive operations (Figure 1, element 104, column 1, lines 32-36), further including:

i. a local memory (Figure 1, element 120);

ii. a plurality of complex arithmetic elements (hereinafter CAE) coupled to one another (Figure 1, element 104), to the local memory (Figure 1, element 120) and to an inter-CAE bus (Figure's 1 and 2, element 114), each of the plurality of CAEs including an arithmetic unit (abstract, column 2, lines 9-16, column 2, line 62-column 3, line 14, Each CAE has a dynamic arithmetic unit.); and

iii. a bus controller coupled to the inter-CAE bus and the connectivity unit (Figure 1, element 106).

8. Cloutier has not taught a plurality of removable complex arithmetic elements. However, Taylor et al. have taught a plurality of removable complex arithmetic units (column 8, lines 35-55, column 10, lines 15-19) for the desirable purpose being able to update the system with faster parts or parts with more resources as needed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the complex arithmetic units of Cloutier, be removable, as taught by Taylor et al., for the desirable purpose of being able to update the system with faster parts or parts with more resources as needed (column 8, lines 35-55, column 10, lines 15-19).

9. Cloutier has not taught each of the plurality of CAEs including a sequencer and the sequencer to sequence data to only the arithmetic unit. However, Pechanek et al. have taught each of a plurality of CAEs including a sequencer (Figure 5, column 5, lines 30-67) and the sequencer to sequence data to only the arithmetic unit (Figure 5-A, Element 206 sequences data to only the arithmetic unit. Figure 6-A, Element 206 sequences data to only element 100 and Element 206' sequences data to only element 100'.) for the desirable purpose of executing multiple independent instruction streams throughout the entire system simultaneously (Column

6). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have each of the plurality of CAEs of Cloutier include a sequencer and the sequencer to sequence data to only the arithmetic unit, as taught by Pechanek et al, so that multiple independent programs are executed in parallel.

10. Referring to claim 2, Cloutier has taught the re-targetable communication processor according to claim 1, as described above, and the plurality of CAEs further comprising:

a. a CAE memory to store data for the mathematically intensive operations (Figure 1, element 120);

b. a data router coupled to the CAE memory (FPGA's inherently contain data router to route data);

c. the arithmetic unit, coupled to the CAE memory and the data router, to execute operations in accordance with the control information (abstract, column 2, lines 62-67, column 3, lines 33-39); and

d. the data router to route data to the sequencer and the CAE memory and to facilitate communications among the CAEs in the scaleable functional unit (Figure 2, The data router inherently routes data to the devices over, north, south, east, west, 114, 118, and data lines.).

11. Referring to claim 3, Cloutier has taught the re-targetable communication processor according to claim 2, as described above, and the CAE memory further comprising: two banks of separately addressable data memories (Figure 1, Each memory is separately addressable.).

12. Referring to claim 4, Cloutier has taught the re-targetable communication processor according to claim 3, as described above, and the arithmetic unit further comprising:

a. a register file to accept data from the data memories (column 2, lines 53-61, column 3, lines 15-22); and

b. a plurality of multiplier-accumulator engines, coupled to one another, to the register file and to the data memories, to operate on the mathematically intensive operations (column 8, lines 56-59).

13. Referring to claim 6, Cloutier has taught the re-targetable communication processor according to claim 5, as described above, and the multiplier further including a programmable shifter (column 8, lines 52-57).

14. Referring to claim 7, Cloutier has taught the re-targetable communication processor according to claim 1, as described above, and the CAEs are coupled to one another via an east port, a west port and the inter-CAE port (Column 2, lines 45-53, Figure 2).

15. Referring to claim 8, Cloutier has taught the re-targetable communication processor according to claim 1, as described above, and further including a micro-controller core coupled to the connectivity unit (Figure 1, element 108).

16. Referring to claim 9, Cloutier has taught the re-targetable communication processor according to claim 2, as described above, and wherein a first delay introduced by the sequencer matches a second delay introduced by the arithmetic unit (FPGA's inherently run in lock step with the controller, or sequencer.).

17. Claim 10 has nothing over claim 1 and is therefore rejected for the same reasons as set forth in claim 1.

18. Claim 11 has nothing over claim 2 and is therefore rejected for the same reasons as set forth in claim 2.

19. Claim 12 has nothing over claim 3 and is therefore rejected for the same reasons as set forth in claim 3.

20. Claim 13 has nothing over claim 4 and is therefore rejected for the same reasons as set forth in claim 4.

21. Claim 15 has nothing over claim 6 and is therefore rejected for the same reasons as set forth in claim 6.

22. Claim 16 has nothing over claim 2 and is therefore rejected for the same reasons as set forth in claim 7.

23. Claim 17 has nothing over claim 9 and is therefore rejected for the same reasons as set forth in claim 9.

24. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloutier, US Patent 5,892,962, in view of Taylor et al., US Patent 5,603,043, Morton, US Patent 6,088,783, and Pechanek et al., US Patent 5,682,491.

25. Referring to claim 5, Cloutier has taught the re-targetable communication processor according to claim 4, as described above. Cloutier has not taught the multiplier-accumulator engine further comprising: a. a pre-adder to generate a first sum by adding data from the register file and the data memory; b. a multiplier to generate a multiplier output by multiplying data from the data memories or the first sum; c. an accumulator to generate a second sum by adding the multiplier output or data from the data memories; and d. a data packing block to configure the second sum into a pre-defined format.

26. However, Morton has taught the multiplier-accumulator engine further comprising:

a. a pre-adder to generate a first sum by adding data from the register file and the data memory (Figure 8, element 809);

b. a multiplier to generate a multiplier output by multiplying data from the data memories or the first sum (Figure 8, element 812);

c. an accumulator to generate a second sum by adding the multiplier output or data from the data memories (figure 8, element 812); and

d. a data packing block to configure the second sum into a pre-defined format (Column 25, line 59-column 26, line 23, 16-bit portions).

27. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the multiplier-accumulator engine of Cloutier, be configured like that of Morton, as described above, for the desirable purpose of allowing quick multiply/accumulate operations on the data (Column 25, line 59-column 26, line 23).

28. Claim 14 has nothing over claim 5 and is therefore rejected for the same reasons as set forth in claim 5.

29. Claims 18-21 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloutier, US Patent 5,892,962, in view of Taylor et al., US Patent 5,603,043, Treiber et al., US Patent 6,324, 062, and Pechanek et al., US Patent 5,682,491.

30. Referring to claim 18, Cloutier has taught a computer system, comprising:

a. a microprocessor (Column 2, lines 39-44, Host) coupled to a system bus (Figure 1, element 122);

b. a system controller coupled to the system bus (Column 2, lines 39-44); and

c. an input/output controller hub (Figure 1, element 106), coupled to the system controller and coupled to an input/output bus (Figure 2, element 114);

d. and coupled to the input/output bus, further including:

e. a re-targetable communication system, comprising:

i. a connectivity unit (Figure 1, element 106);

ii. a digital signal processing core coupled to the connectivity unit (Figure 1, element 104, one of the FPGA's is a digital signal processor);

iii. a plurality of scaleable functional units, coupled to the connectivity unit, to execute mathematically intensive operations (Figure 1, element 104), further including:

(1) a local memory (Figure 1, element 120);

(2) a plurality of complex arithmetic elements (hereinafter CAE) coupled to one another (Figure 1, element 104), to the local memory (Figure 1, element 120) and to an inter-CAE bus (Figure's 1 and 2, element 114), each of the plurality of CAEs including a sequencer and an arithmetic unit (abstract, column 2, lines 9-16, column 2, line 62-column 3, line 14, Each CAE has a dynamic arithmetic unit.); and

(3) a bus controller coupled to the inter-CAE bus and the connectivity unit (Figure 1, element 106).

31. Cloutier has not taught a plurality of removable complex arithmetic elements. However, Taylor et al. have taught a plurality of removable complex arithmetic units (column 8, lines 35-55, column 10, lines 15-19) for the desirable purpose being able to update the system with faster

parts or parts with more resources as needed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the complex arithmetic units of Cloutier, be removable, as taught by Taylor et al., for the desirable purpose of being able to update the system with faster parts or parts with more resources as needed (column 8, lines 35-55, column 10, lines 15-19).

32. Futhermore, Cloutier has not taught that the re-targetable communication system is an add-in card. However, Treiber et al. have taught a processor system that is removable so that the system does not have to be powered down while swapping in/out a part, thereby enabling hot swapping (abstract, column 8, lines 10-14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the re-targetable communication system of cloutier be implemented as an add in card, for the desirable purpose of allowing hot swapping to occur without an overall system power down.

33. Cloutier has not taught each of the plurality of CAEs including a sequencer and the sequencer to sequence data to only the arithmetic unit. However, Pechanek et al. have taught each of a plurality of CAEs including a sequencer (Figure 5, column 5, lines 30-67) and the sequencer to sequence data to only the arithmetic unit (Figure 5-A, Element 206 sequences data to only the arithmetic unit. Figure 6-A, Element 206 sequences data to only element 100 and Element 206' sequences data to only element 100'.) for the desirable purpose of executing multiple independent instruction streams throughout the entire system simultaneously (Column 6). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have each of the plurality of CAEs of Cloutier include a sequencer and

the sequencer to sequence data to only the arithmetic unit, as taught by Pechanek et al, so that multiple independent programs are executed in parallel.

34. Claim 19 has nothing over claim 2 and is therefore rejected for the same reasons as set forth in claim 2.

35. Claim 20 has nothing over claim 3 and is therefore rejected for the same reasons as set forth in claim 3.

36. Claim 21 has nothing over claim 4 and is therefore rejected for the same reasons as set forth in claim 4.

37. Claim 23 has nothing over claim 6 and is therefore rejected for the same reasons as set forth in claim 6.

38. Claim 24 has nothing over claim 7 and is therefore rejected for the same reasons as set forth in claim 7.

39. Claim 25 has nothing over claim 8 and is therefore rejected for the same reasons as set forth in claim 8.

40. Claim 26 has nothing over claim 9 and is therefore rejected for the same reasons as set forth in claim 9.

41. Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cloutier, US Patent 5,892,962, in view of Taylor et al., US Patent 5,603,043, Treiber et al., US Patent 6,324,062, Morton, US Patent 6,088,783, and Pechanek et al., US Patent 5,682,491.

42. Claim 22 has nothing over claim 5 and is therefore rejected for the same reasons as set forth in claim 5.

Response to Arguments

43. Applicant's arguments with respect to claims 1-26 have been considered and are addressed in the ground(s) of rejection above.

Conclusion

44. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

45. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

46. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100